SYSTEM FOR, AND METHOD OF, PROCESSING QUADRATURE AMPLITUDE MODULATED SIGNALS

Abstract of the Disclosure

Analog signals encoded with quadrature amplitude modulation (QAM) pass through a coaxial cable at a particular baud rate. These signals have a carrier frequency individual to the TV station being received. They are mixed with signals from a variable frequency oscillator to produce signals at a particular intermediate frequency (IF). An analog-digital converter (ADC) converts the IF signals to corresponding digital signals which are demodulated to produce two digital signals having a quadrature phase relationship. After being filtered and derotated, the digital signals pass to a symmetrical equalizer including a feed forward equalizer (FFE) and a decision feedback equalizer (DFE) connected to the FFE in a feedback relationship. The DFE may include a slicer providing amplitude approximations of increasing sensitivity at progressive times. Additional slicers in the equalizer combine the FFE and DFE outputs to provide the output data without any of the coaxial cable noise or distortions. The equalizer outputs and initially the derotation outputs, and the slicer outputs, servo (1) the oscillator frequency to obtain the IF frequency, (2) the ADC sampling clock to obtain the digital conversion at a rate related to the particular baud rate and (3) the derotator. The servos may have (1) first constants initially after a change in the station selection and (2) second time constants thereafter. The ADC gain is also servoed (1) initially in every ADC conversion and

(2) subsequently in every nth ADC conversion where n= integer > 1. The above recover the QAM data without any of the coaxial cable noise or distortions.

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This invention relates to systems for, and methods of, recovering digitally modulated television signals from the noise and distortion in coaxial cables. More particularly, this invention relates to systems for, and methods of, recovering quadrature amplitude modulated signals from the noise and distortion in coaxial cables. In these systems and methods, quadrature amplitude modulation is used to transmit the television information. The systems and methods of this invention use digital techniques to recover the quadrature amplitude modulated signals from the noise and distortion in the coaxial cables.

Modern digital telecommunication systems are operating at ever-increasing data rates to accommodate society's growing demands for information exchange. However, increasing the data rates, while at the same time accommodating the fixed bandwidths allocated by the Federal Communications Commission (FCC), requires increasingly sophisticated signal processing techniques. Since low cost, small size and low power consumption are important in the hardware implementations of such communications systems, custom integrated-circuit solutions are important in achieving these goals.

Next-generation digital television systems such as proposed cable television (CATV) and high-definition television (HDTV) will rely on transceivers to deliver data at

rates in excess of thirty megabits per second (30 Mb/s). Quadrature amplitude modulation (QAM) techniques, used in high-speed modems and digital radio systems, represent a promising transmission format for CATV and HDTV systems. In quadrature amplitude modulation (QAM) systems, a pair of amplitude modulated signals having a quadrature (90°) phase relationship to each other are summed to transmit the television signals through the coaxial cable.

There are problems in the use of quadrature amplitude modulation for CATV and HDTV systems. One significant problem is that a considerable amount of noise and distortion is generated in the coaxial cables. Such distortion may result in CATV systems in part from impedance mismatches and reflections from unterminated stubs. In HDTV systems, the distortion may result in part from multi-path reflections. Such distortion is so significant that it impairs a good reception of the television signals.

Until now, analog systems have been proposed to recover the quadrature amplitude modulated data from the analog CATV and HDTV signals in the coaxial cables. Such systems have been disadvantageous because they have not been able to eliminate a significant amount of the noise and distortion in the coaxial cables. Even with their inefficiencies, they have required large amounts of power and considerable space.

This invention recovers the quadrature amplitude modulated data by using digital techniques. The current embodiment of the invention uses only three (3) integrated circuit chips to provide such recovery. The invention recovers the quadrature amplitude modulated data while eliminating substantially all of the noise and distortion in the coaxial cables. The invention also provides for an increased speed of operation, thereby being capable of handling television signals transmitted at increased baud rates. The three (3) integrated circuit chips consume a relatively low amount of power and occupy a relatively small space. Steps are now being taken to provide in a single chip the system now provided in three (3) chips. This chip will occupy even less space and consume less power than the three (3) chip system.

In one embodiment of the invention, analog signals encoded with quadrature amplitude modulation (QAM) pass through a coaxial cable at a particular baud rate. The analog signals have a carrier frequency individual to the TV station being received. These signals are mixed with signals from a variable frequency oscillator to produce signals at a particular intermediate frequency (IF). An analog-digital converter (ADC) converts the intermediate frequency (IF) signals to corresponding digital signals which are demodulated to produce two digital signals having a quadrature phase relationship.

After being filtered and derotated, the two digital signals pass to a symmetrical equalizer including a feed forward equalizer (FFE) and a decision feedback equalizer (DFE) connected to the FFE in a feedback relationship. The DFE may include a slicer providing amplitude approximations of increasing sensitivity at progressive times. Additional slicers in the equalizer combine the FFE and DFE outputs to provide the output data without any of the coaxial cable noise or distortions.

The equalizer outputs and initially the derotation outputs, and the slicer outputs, servo (1) the oscillator to obtain the IF frequency, (2) the ADC sampling clock to obtain the digital conversion at a rate having a particular relationship to the particular baud rate and (3) the derotator. The servos may have (1) first constants initially after the selected TV channel is changed and (2) second time constants thereafter. The ADC gain is also servoed (1) initially in every ADC conversion and (2) subsequently in every nth ADC conversion where n= integer > 1. The above recover the QAM data without any of the noise or distortion in the coaxial cable.

In the drawings:

Figure 1 is a diagram schematically illustrating a system for transmitting analog television signals (video and audio) from a selected one of a number of channels or stations

through a coaxial cable for reception by a subscriber, the analog signals having been encoded using quadrature amplitude modulation;

Figures 2A and 2B collectively constitute a circuit diagram, primarily in block form, of a system constituting one embodiment of the invention for recovering the quadrature amplitude modulated signals from the noise and distortion in the coaxial cable;

Figure 3 is a schematic diagram illustrating how a cosine signal is generated in one of the stages of Figure 2 on a digital basis;

Figure 4 is a simplified schematic diagram illustrating how the derotator and equalizer included in the embodiment of Figures 2A and 2B produce an undistorted quadrature amplitude modulation constellation corresponding to the quadrature amplitude modulation signal generated by the transmitting station;

Figure 5 is a circuit diagram, primarily in block form, illustrating in additional detail data and error slicer stages in an equalizer chip shown in Figure 2A;

Figure 6 is a chart further illustrating the possible output values of the slicer when operating in a 64-QAM mode;

Figure 7 is a schematic diagram illustrating how certain closed loop servos included in the embodiment of Figures 2A and 2B operate when the equalizer chip shown in

Figure 2 provides a QAM constellation with a phase rotation displaced from the QAM constellation transmitted through the coaxial cable by the selected station;

Figure 8 is a curve further illustrating how the closed loop servos included in the embodiment of Figures 2A and 2B operate when the equalizer chip shown in Figure 2A provides a QAM waveform with a sampling phase displaced from the ideal sampling phase generated by the transmitting station; and

Figure 9 illustrates how filters included in the equalizer chip shown in Figure 2 produce different parts of the composite QAM signal which is free of the distortion in the coaxial cable.

In one embodiment of the invention, a plurality of television stations or channels 10 (Figure 1) are provided to transmit television signals (video and audio) through a coaxial cable 12 to a receiver (not shown). Each of the television channels 10 provides a carrier signal at a frequency individual to such channel. The carrier frequency for the lowest one of the stations or channels 10 may be approximately thirty (30) megahertz (30 MHz) and the carrier frequency for the highest one of the stations or channels may have a value of approximately seven hundred and fifty megahertz (750 MHz). The separation in frequency between adjacent pairs of channels may be approximately six megahertz (6 MHz).

The television signals (video and audio) are digitally compressed and encoded and transmitted through the coaxial cable 12 using quadrature amplitude modulation. The television signals modulated as described above are transmitted through the coaxial cable 12 at a particular baud rate. The signals may be compressed by an amount depending upon the baud rate.

A system as described above is well known in the art. Such a system is being proposed to transmit cable television (CATV) signals and is proposed for use to transmit high definition television signals (HDTV) through a coaxial cable such as the cable 12.

As the modulated television signals are transmitted through the coaxial cable 12, noise and distortion develop in the coaxial cable. The distortion may develop from a number of factors. For example, the distortion may develop in cable television systems from impedance mismatches and reflections from unterminated stubs. In high definition broadcast television signals, the distortion may result from multi-path reflections. The distortion in the coaxial cable 12 is so significant that it may prevent the QAM signal from being recovered. The QAM signal has to be recovered in order for the television signals (audio and video) to be processed in the set-top box.

This invention provides a system for, and method of, processing the analog signals in the coaxial cable 12 for any selected one of the individual channels 10 to recover the quadrature amplitude modulated data for such channel from the noise and distortion in the coaxial cable. When the quadrature amplitude modulated data has been recovered by the system of this invention, the television signals (video and audio) for the selected channel 10 can be processed by known techniques to obtain the image and the sound being transmitted in that channel.

The analog signals in the coaxial cable 12 are introduced to a mixer/filter 16 and an oscillator 14 having a variable frequency. The oscillator 14 may preferably be a voltage controlled oscillator whose frequency is varied in accordance with variations in the voltage introduced to the oscillator. As will be described subsequently, the voltage introduced to the oscillator 14 is varied to have the frequency of the oscillator be separated by an intermediate frequency (IF) such as five megahertz (5MHz) from the individual one of the channels or stations 12 selected at any instant. These signals are mixed in a mixer/filter 16 with the carrier signals in the coaxial cable 12 to produce the intermediate frequency (IF) signal of five megahertz (5MHz).

The IF analog signals are then introduced to an analog-to-digital converter 18 (Figures 1 and 2A). As will be

seen subsequently, the converter 18 operates on the analog signals at four (4) times the baud rate of the selected one of the channels 10 and converts the analog signals to digital signals at this baud rate. The digital signals are then introduced to a pair of multipliers 20 and 22 in Figure 2A. The multiplier 20 multiplies the digital signals by a cosine function and the multiplier 22 multiplies the digital signals by a sine function. The multiplication by the cosine function occurs from a phase standpoint at progressive 90° intervals. Thus the multiplication occurs with successive digital values of +1,0,-1,0,+1,0,-1,0, etc. In like manner, the multiplication of the digital signals by the sine function occurs at 90° intervals as by successive digital values of 0,+1,0,-1,0,+1, 0,-1, etc. The sine and cosine functions formulated as specified above are shown in Figure 3. The sine function is shown in a solid line and the cosine function is shown in broken lines.

Since the multiplication by each of the sine and cosine functions occurs at four times the baud rate, each of the multipliers 20 and 22 produces signals at a frequency four (4) times the baud rate. The signals from the multipliers 20 and 22 are respectively introduced to canonic signed digit low pass filters 24 and 26. Such low pass filters are well known in the art. For example, they are disclosed in an article entitled "A 200 MHz, All-Digital QAM Modulator and Demodulator in 1.2-um CMOS for Digital Radio Applications" written by

Bennett C. Wong and Henry Samueli and published in the IEEE Journal of Solid-State Circuits in December 1991. One advantage of such a low pass filter is that it employs a series of adders rather than multipliers as in other filters. Adders are distinctly advantageous over multipliers because they are considerably less complicated in construction and operation than multipliers. This provides for simplicity in the construction and operation of the low pass filters and for a minimal dissipation of power in the filters.

The frequency of the signals from the low pass filters 24 and 26 is divided by two (2) in a pair of stages 28 and 30. The dividers 28 and 30 are disclosed in the article specified in the previous paragraph. After such division, the frequency of the digital signals is still two (2) times the baud rate of the quadrature amplitude modulated data in the coaxial cable 12. The signals from the dividers 28 and 30 are then introduced to a phase derotator 32. The phase derotator 32 is considered to be one (1) of the novel features of this invention. The phase derotator 32 multiplies the baseband digital signals from the dividers 28 and 30 by the trigonometric functions sin $\emptyset$ and cos $\emptyset$. These trigonometric functions have a sampling frequency corresponding to that of the digital signals from the dividers 28 and 30. The functions cosine $\emptyset$ and sine $\emptyset$ are supplied by a stage 34.

If the output from the divider 28 is considered as I

and the output from the divider 30 is considered as Q, the multiplications provided in the derotator 32 may be indicated as

$$I \cos \phi$$

$$Q \sin \phi$$

$$I \sin \phi$$

$$Q \cos \phi$$

The multiplicands listed above may be combined in pairs as

$$I \cos \phi - Q \sin \phi \text{ and}$$

$$I \sin \phi - Q \cos \phi$$

to produce outputs on lines 36 and 38 of the phase derotator.

If the phases of the pairs of the signals $I \cos \phi - Q \sin \phi$ and $I \sin \phi - Q \cos \phi$ do not match the phases of the transmitted QAM constellation, there will be a rotation of the signals. This may be seen from Figure 4 where four (4) columns and four (4) rows are shown and where Q is shown on the horizontal axis and I is shown on the vertical axis. When the phases of I and Q are properly aligned, the QAM constellation will have the relationship shown in Figure 4. In this relationship, the I values have a perpendicular relationship and are stationary and the Q values have a horizontal relationship and are stationary. If the phases of I and Q are not properly aligned with the transmitted QAM constellation, the I and Q constellation will spin at a rate dependent upon the differences in phase between the I and Q constellation on the one hand and the transmitted QAM

constellation in the coaxial cable 12 on the other hand.

The stages 20, 22, 24, 26, 28, 30 and 32 have been included in an integrated circuit chip generally indicated at 34 in Figure 2A. This chip is designated in Figure 2A as QAM DEMOD CHIP and is shown in broken lines. The signals from the phase derotator 32 in the integrated circuit chip 34 pass through the lines 36 and 38 to a feed forward equalizer (FFE) 40 in an integrated circuit chip generally indicated at 42. The chip 42 is designated in Figure 2 as an "EQUALIZER CHIP" and is shown in broken lines. A suitable feed forward equalizer 40 is disclosed in an article entitled "A 100 MHz, 5MBaud Decision Feedback Equalizer for Digital Television Applications" written by Robindra B. Joshi and Henry Samueli and published in the IEEE International Solid-States Circuits Conference on February 16, 1994. The feed forward equalizer 40 may perform either a T-spaced function or a T/2-spaced function.

The rate of occurrence of the outputs from the feed forward equalizer 40 is divided in the chip 42 by a pair of stages 44 and 46. Each of these divisions is by a factor of two (2). This causes the digital signals from the dividers 44 and 46 to have the baud rate of the analog signals introduced to the converter 18. The signals from the dividers 44 and 46 are respectively introduced to adders 48 and 50 as are outputs

from a decision feedback equalizer 52. The adders 48 and 50 and the decision feedback equalizer 52 are included in the equalizer chip 42. The decision feedback equalizer 52 and the combination of the stages in the equalizer chip 42 are considered to be new to this invention.

The adder 48 adds the outputs of the feed forward equalizer 40 and the decision feedback equalizer 52 to provide an output which is introduced to a slicer 54. This addition may be seen from Figure 9. As will be seen, a composite signal generally indicated at 51 is shown as being comprised respectively of left and right halves 51a and 51b. The feed forward equalizer 40 may be considered to correct for distortions in the left half 51a of the composite signal 51 and the decision feedback equalizer 52 may be considered to correct for distortions in the right half 51b of the composite signal 51. The adder 48 accordingly provides the binary value of the composite signal 51.

The outputs from the adders 48 and 50 are shown in Figure 2A as being respectively introduced to a pair of slicers 54 and 56. Slicers such as the slicers 54 and 56 are considered to be known in the art. Each of the slicers 54 and 56 operates to provide a plurality (such as eight (8)) of progressive values and to determine the particular one of the eight (8) values closest to the output of the associated adder. For example, the slicer 54 selects a particular one of

the eight (8) values closest to the output of the adder 48 and then provides this output on a line 58. Similarly, the slicer 56 selects a particular one of the eight (8) values closest to the output of the adder 50 and then provides this output on a line 60. The slicers 54 and 56 are included in the integrated circuit chip 42.

As will be seen in Figure 2A, the stages on the integrated circuit chip 42 are symmetrical with respect to the I and Q channels. The symmetry is provided because of the symmetrical relationship of the stages 44, 48 and 54 between the equalizers 40 and 52 and the stages 46, 50 and 56 between the equalizers. The symmetrical relationship of the stages in the integrated circuit chip 42 facilitates an optimal detection of the quadrature amplitude modulated signals on the lines 58 and 60 with much less complexity than an asymmetrical structure. The symmetrical structure is practical when the analog-digital converter 18 operates on the IF signal. When the analog-digital converter operates on the baseband I and Q signals, an asymmetrical structure is required. This increases the complexity of the hardware.

Figure 5 illustrates certain of the stages in Figure 2A in additional detail. Figure 5 shows the adder 48 and the slicer 54 also shown in Figure 2A. Figure 5 also shows the output from the feed forward equalizer 40 on a line 62 and the output from the decision feedback equalizer 52 on a line 64,

both of these outputs being introduced to the adder 48. As in Figure 2A, the output of the adder 48 is shown as being introduced to the slicer 54. The output of the adder 48 is also shown in Figure 5 as being introduced to the input of a slicer 66 which is included in the decision feedback equalizer 52 shown in broken lines in Figure 5. The slicer 66 also receives a control input on a line 68. The output of the slicer 66 is introduced to a stage 70 which determines the difference between the output of the slicer 66 and the output of the adder 48. The output of the stage 70 is introduced on a line 71 to both the feed forward equalizer 40 and the decision feedback equalizer 52 also shown in Figure 2A. This output may be considered to constitute the error feedback from the slicer 66 to the feed forward equalizer 40 and the decision feedback equalizer 52 in Figure 2A.

The control line 68 receives successive binary indications from a microprocessor 72 (Figure 2B) of two (2), four (4), eight (8) and sixteen (16) binary values. These respectively represent the square roots of four (4), sixteen (16), sixty four (64) and two hundred and fifty six (256). When the control line 68 in Figure 5 receives a binary indication of two (2), the slicer 66 selects the binary value from the adder 48 closest to the two (2) progressive binary values in the slicer 66 and substitutes the closest of these two (2) values in the slicer 66 as the output from the slicer 66.

After a fixed period of time preset into the microprocessor 72, the slicer 66 provides four (4) progressive binary values and determines which one of these four (4) progressive binary values is closest to the binary value now provided as the output from the slicer. After an additional fixed period of time preset by the microprocessor 72, the slicer 66 again increases the number of progressive binary values, this time to eight (8). The slicer 66 then determines the individual one of the eight (8) progressive binary values closest to the adjusted input to the slicer 66 and selects this individual one of the progressive binary values as the new adjusted output from the slicer 66. If the receiver is operating in the 256-QAM mode, then, after another fixed period of time preset by the microprocessor 72, the slicer 66 again repeats this procedure, but this time with sixteen (16) progressive values in the slicer 66.

In this way, the slicer 66 initially provides a coarse control and, in subsequent time periods preset by the microprocessor 72, provides controls of progressively increasing sensitivity. These controls of progressively increasing sensitivity are fed by the slicer 66 to the stage 70, which produces the error signal that is fed back to the feed forward equalizer 40 and the decision feedback equalizer 52 to control the operation of coefficient updating loops in the equalizers. Upon each such feedback, the feed forward equalizer 40 and the decision feedback equalizer 52 adjust the

values of the binary filter coefficients in the equalizers to provide an output of progressively increasing accuracy from the slicer 54.

Although the discussion above has centered specifically on the adder 48, the slicer 66 and the slicer 54, it will be appreciated that similar operations may be provided for a slicer (corresponding to the slicer 66) associated with the adder 50 and the slicer 56 to provide an output of progressively increasing accuracy from the slicer 56. As a result, the slicers 54 and 56 progressively provide, at successive instants of time, in-phase (I) and quadrature (Q) data estimates which progressively approach the values of the quadrature amplitude modulated data in the coaxial line 12.

In providing at progressive instants of time the outputs discussed in the previous paragraph, the slicer 66 in Figure 5 provides at progressive instants of time two (2), four (4), eight (8) and sixteen (16) binary levels. The corresponding slicer associated with the adder 50 provides similar numbers of binary levels at progressive instants of time. Since the two (2) slicers respectively represent I and Q, they provide at successive instants of time four (4), sixteen (16), sixty four (64) and two hundred and fifty six (256) possible output pairs. This may be seen from the representation shown in Figure 4 for the case of sixteen (16) outputs.

There are a number of closed loop servos which enhance the response of the system constituting this invention. One of these is indicated generally at 74 in Figure 2B. It provides an automatic gain control for the analog signals introduced to the analog-digital converter 18. As will be appreciated, it is desirable to regulate the gain of the analog signals before they are converted to digital signals by the converter 18. One reason is that the amplitude of the analog signals at each instant affects the characteristics of the television information. The automatic gain control (AGC) servo 74 includes an AGC discriminant stage 76, an accumulator stage 78, a multiplier 80 and a digital-to-analog converter 82. The converter 82 may be a delta-sigma converter well known in the art. Although the stages 74, 76, 78, 80 and 82 may be considered to be individually known in the art, they are not known in the environment included in this invention for regulating the gain of the input to the analog-digital converter 18 in this invention.

The AGC discriminant stage 76 initially provides a determination of the digital value (after conversion from analog) at a rate four (4) times the rate of the baud samples. This stage provides a close regulation of the gain in the analog signals. After a fixed time preset by the microprocessor 72, the AGC discriminant stage 76 provides a determination of the digital value (after conversion from analog) in every nth baud sample where n is an integer greater

than one (1) and is preset by the microprocessor 72 (Figure 2B).

The AGC discriminant stage 76 is able to operate in every nth sample because the stage has previously provided a strong (or coarse) regulation by determining and regulating the digital value at a rate four (4) times the rate of the baud samplings. Providing the determination in every nth baud sample after this initial strong (or coarse) regulation is desirable because it minimizes the consumption of power and because the circuitry for providing the determination in every nth baud sample is simpler than the circuitry for providing the determination at a rate four (4) times the rate of the baud samples.

The output from the AGC discriminant stage 76 is introduced to the accumulator 78 which operates to sum and average this output with the previous outputs from the stage 76. The multiplier 80 then multiplies the output from the accumulator 78 by a constant value b_0 preset by the microprocessor 72. The constant b_0 is initially set by the microprocessor 72 at a first fixed value. This first value for the constant b_0 is set so that the servo 74 can provide strong (or coarse) adjustments after the television station or channel 10 desired to be viewed has been changed.

After a fixed period of time preset by the

microprocessor 72, the constant b_0 is changed by the microprocessor 72 to a second value. This second value of the constant b_0 provides for a weaker regulation than the first value of the constant b_0. This weaker regulation is quite satisfactory because of the previously strong (or coarse) regulation during the period of the first value of the constant. The output of the multiplier 80 is converted to an analog value by the converter 82. This analog value is used to regulate the gain of the analog signals introduced to the input to the analog-digital converter 18.

Another closed loop servo, generally indicated at 84 in Figure 2B, corrects for the frequency of the variable frequency oscillator 14 (e.g. voltage controlled oscillator) to provide the oscillator with a frequency which differs from the carrier frequency for the selected station 10 by the intermediate frequency of five megahertz (5 MHz). In this way, a constant intermediate frequency can be provided regardless of which one of the stations 10 in the plurality is selected. The servo 84 includes an intermediate frequency (IF) carrier phase detector 86 having inputs respectively connected initially to the two (2) output lines 36 and 38 from the derotator 32 in Figure 2A. The output lines 36 and 38 are respectively designated as IDEROT and QDEROT in Figure 2A. Inputs to the intermediate carrier phase detector 86 are also